WHAT IS CLAIMED IS:

1. A semiconductor chip comprising:

a semiconductor substrate comprising an active region;

a first structure formed in the active region, the first structure being fully silicided; and

at least one dummy silicide structure.

2. The semiconductor chip of claim 1 wherein the first structure is a transistor gate electrode of a transistor.

3. The semiconductor chip of claim 2 wherein the transistor further comprises a gate dielectric underlying the first structure, the gate dielectric comprising a high permittivity dielectric selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthalum oxide, cerium oxide, titanium oxide, and tantalum oxide.

4. The semiconductor chip of claim 1 wherein the dummy silicide structure is located in the active region.

5. The semiconductor chip of claim 1 wherein the dummy silicide structure is located in an isolation region separate from the active region.

6. The semiconductor chip of claim 1 wherein the first structure and dummy silicide structure each comprises nickel silicide.

7. The semiconductor chip of claim 1 wherein the first structure and dummy silicide structure each comprises a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.

8. The semiconductor chip of claim 1 wherein the first structure and dummy silicide structure each comprises germanium.

9. The semiconductor chip of claim 1 wherein the semiconductor substrate is a silicon substrate.

10. The semiconductor chip of claim 1 wherein the semiconductor substrate is a semiconductor-on-insulator substrate.

11. The semiconductor chip of claim 1 further comprising a contact etch-stop layer overlying portions of the first structure.

12. The semiconductor chip of claim 1 further comprising a dielectric layer overlying the first structure and dummy silicide structure.

13. An integrated circuit chip comprising:

a substrate having an active region and an isolation region;

a transistor formed on the active region, the transistor having a source region, a drain region, and a fully silicided gate electrode; and

at least one dummy silicide structure.

14. The integrated circuit chip of claim 13 wherein electrical contacts are electrically coupled to the source region, the drain region, and the fully silicided gate electrodes.

15. The integrated circuit chip of claim 13 wherein the dummy silicided structure is located in the active region.

16. The integrated circuit chip of claim 13 wherein the dummy silicided structure is located in the isolation region.

17. The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and dummy silicided structure comprise nickel silicide.

18. The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and dummy silicided structure comprise a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.

19. The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and dummy silicided structure comprise germanium.

20. A method of forming a semiconductor device having a fully silicided structure, the method comprising the steps of:

providing a substrate having an active region and an isolation region;

forming a first polysilicon structure on the substrate;

forming a dummy polysilicon structure on the substrate, the dummy polysilicon structure being an inoperative circuit element;

forming a metal layer over the first polysilicon structure and the dummy polysilicon structure; and

siliciding first polysilicon structure and the dummy polysilicon structure with the metal layer to form a first fully silicided structure and a fully silicided dummy structure.

21. The method of claim 20 wherein the first polysilicon structure is a gate electrode of a transistor.

22. The method of claim 20 wherein the first polysilicon structure is located in the active region.

23. The method of claim 20 wherein the dummy polysilicon structure is located in the inactive region.

24. The method of claim 20 wherein forming the metal layer includes:

forming a dielectric layer over the first polysilicon structure and the dummy polysilicon structure; and

planarizing the dielectric layer such that the first polysilicon structure and the dummy polysilicon structure are exposed.

25. The method of claim 20 wherein the step of siliciding is performed by annealing at a temperature of about 200° C to about 900° C in an ambient comprising nitrogen, helium, argon, or neon.

26. The method of claim 20 wherein the step of forming the dummy silicided structure is performed by forming the dummy silicided structure in the active region.

27. The method of claim 20 the step of forming the dummy silicided structure is performed by forming the dummy silicided structure in the isolation region.

28. The method of claim 20 wherein the first fully silicided structure and the dummy silicided structure comprise nickel silicide.

29. The method of claim 20 wherein the first fully silicided structure and the dummy silicided structure comprise a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.

30. The method of claim 20 wherein the first fully silicided structure and the dummy silicided structure comprise germanium.

31. The method of claim 20 wherein the step of forming the first polysilicon structure and the step of forming the dummy polysilicon structure are performed in the same process step.

32. The method of claim 20 wherein the dummy polysilicon structure is not electrically coupled to an active circuit element.

33. The method of claim 20 wherein the first polysilicon structure is a gate of a transistor.

34. A method of forming a transistor with fully silicided gate electrode, the method comprising the steps of:

providing a substrate having an active region and an isolation region;

forming a gate dielectric over the substrate;

forming a gate electrode and a dummy electrode over the gate dielectric, the gate electrode and the dummy electrode comprising silicon, the dummy electrode being an inactive circuit element;

forming source and drain regions oppositely adjacent the gate electrode to form a transistor;

depositing metal over the gate electrode and dummy electrode; and

siliciding the gate electrode and the dummy electrode with the metal to form a fully silicided gate electrode and a fully silicided dummy electrode.

35. The method of claim 34 wherein the gate electrode is located in the active region.

36. The method of claim 34 wherein the dummy electrode is located in the isolation region.

37. The method of claim 34 wherein depositing metal includes:

forming a dielectric layer over the gate electrode and the dummy electrode; and

planarizing the dielectric layer such that the gate electrode and the dummy electrode are exposed.

38. The method of claim 34 wherein the step of siliciding is performed by annealing at a temperature of about 200° C to about 900° C in an ambient comprising nitrogen, helium, argon, or neon.

39. The method of claim 34 wherein the fully silicided gate electrode and the fully silicided dummy electrode comprise nickel silicide.

40. The method of claim 34 wherein the fully silicized gate electrode and the fully silicized dummy electrode comprise a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.

41. The method of claim 34 wherein the fully silicided gate electrode and the fully silicized dummy electrode comprise germanium.

42. The method of claim 34 wherein the step of forming the gate electrode and the dummy electrode are performed in the same process step.

43. The method of claim 34 wherein the dummy electrode is not electrically coupled to an active circuit element.